REMARKS

The Office Action of June 28, 2007 has been received and its contents carefully considered. An RCE is being filed concurrently to permit further prosecution.

The present Amendment corrects independent claims 1 and 7 to conform to the disclosure in the paragraph at page 9 of the application, lines 8-15. This paragraph provides that the resistance of the surge absorption element during breakdown operation of the surge absorption element is smaller than the resistance of the transistor (not the surge absorption element) during breakdown operation of the transistor.

The present Amendment also revises independent claim 7 so that it now specifies only one transistor, and so that it requires all of the conditions (instead of "at least one") to be fulfilled.

In addition, the present Amendment adds new dependent claims 10 and 11. These new dependent claims are similar to claims 8 and 9 but depend from claim 7 instead of claim 1.

The present Amendment also changes the "surge absorption element" that was previously recited in claim 1 to "a vertical diode formed in a diode well," and adds that "said diode has a breakdown voltage that is established at a desired value as a function of a junction depth of said diode, an impurity concentration in said well, a resistivity of said substrate, and a thickness of said substrate." These revisions are supported (for example) by the passage at page 4, lines 17-19; by the passage at page 7, line 15 to page 8, line 7; and by the passage at page 11, line 21 to page 12, line 8.

Finally, the present Amendment revises dependent claims 2-6 in order to conform to the changes that have been made to claim 1.

The Office Action rejects the claims for obviousness on the basis of US patent 6,365,932 to Kouno et (which will hereafter be called simply "Kouno"). The rejection is respectfully traversed for the reasons discussed below.

Claim 1 now recites a "vertical diode formed in the diode well." A vertical diode has a pn junction that extends primarily in a longitudinal direction (see, for example, the vertical diode 30 that is shown in Figure 3 of the present application's drawings). Kouno does not disclose a vertical diode. Kouno's surge absorber is a horizontal-type semiconductor device, in which the pn junction is provided primarily in a transverse direction.

Claim 1 now also recites that the diode "has a breakdown voltage that is established at a desired value as a function of a junction depth of said diode, an impurity concentration in said well, a resistivity of said substrate, and a thickness of said substrate." Kouno neither discloses nor suggests using such factors in order to establish the breakdown voltage of a diode at a desired value. Indeed, the "junction depth of said diode" does not even apply to Kouno's horizontal-type surge absorber.

It has also been mentioned already that the independent claims have been corrected to provide that the resistance of the surge absorption element during its breakdown operation is smaller than the resistance of the transistor during its breakdown operation. On page 3, the Office Action takes the position that what was recited in claim 1 previously would have been obvious "since one would not want the surge protection (surge absorption) affecting normal operations of the transistor, and hence, one would want current flow through the absorption element only when there is a surge and not otherwise." With a current formulation of the independent claims, surge protection would not affect normal operation of the transistor.

It is respectfully submitted that what an ordinarily skilled person would want is a surge absorption element that goes into breakdown operation at a voltage lower than the transistor goes into breakdown operation, and that is sufficiently robust that it could handle the current expected during an ESD event without being destroyed. With these two concerns in mind, the ordinarily skilled person would have had no reason to even consider the resistance of the surge absorption element during breakdown operation or the resistance of the transistor during breakdown operation. The ordinarily skilled person would certainly have had no reason to think that it would be desirable for the resistance of the surge absorption element during breakdown operation to be smaller than the resistance of the transistor during breakdown operation of the transistor.

The second condition recited in claim 1, and also one of the conditions recited in independent claim 7, is that "a secondary breakdown current of said surge absorption element is larger than a secondary breakdown current of said transistor." The Office Action comments on page 3 that, "as the absorption element is intended to protect the transistor, ...one would not want it to enter into thermal runaway sooner...". It is respectfully submitted, though, that an ordinarily skilled person would likely think that the surge absorption element should be selected so as to keep the transistor from undergoing secondary breakdown in the first place. Without secondary breakdown of the transistor, the ordinarily skilled person would have had no reason to concern himself with the secondary breakdown current of the transistor.

Accordingly, it is respectfully submitted that the invention defined by claim 1 is patentable over the Kouno. Independent claim 7 recites various relationships, including the relationships set for the in the first two "wherein" clauses of claim 1, so claim 7 is

patentable on the basis of these two relationships for the reasons discussed above, even apart from the further relationships that are recited in claim 7.

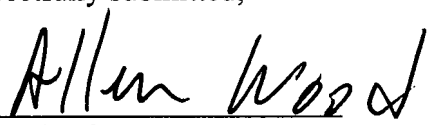
At the bottom of page 3 and top of page 4, the Office Action comments that it is not understood how the first and second conditions of claim 1 (now the first and second "wherein" clauses of claim 1) translate into avoidance of "surplus surge-absorption capacity," and that arguments presented in the last Amendment appear to be mere opinions without probative value. These comments call for a response, which is as follows: An ordinarily skilled person would want to do two things. He would want to make sure that the surge absorption element enters avalanche breakdown before the transistor that it protects, and to also make sure that the surge absorption element is robust enough to withstand the current associated with an ESD event (of some anticipated voltage) without being fried. The ordinarily skilled person would appreciate that the transistor protected by a surge absorption element would be jeopardized if the surge absorption element is damaged due to excessive current. In view of these two concerns of the ordinarily skilled person, the practical thing for the ordinarily skilled person to do would be to take no chances, and to employ a surge absorption element that is physically large enough that it would certainly be able to handle a current associated with an ESD event of some designed-for voltage.

The inventors have undertaken a study of what is necessary in order for the surge absorption element to do its job. This permits them to avoid wasted space on a chip by limiting the size of the surge absorption element to what is really needed. It is no longer necessary to fabricate more surge absorption capacity than is needed just to make sure that there is enough.

The remaining claims depend from the independent claims discussed above and recite additional limitations to further define the invention. They are therefore automatically patentable along with their independent claims. It is nevertheless noted that the Office Action, at the bottom of page 3, takes the position that the limitations of claims 8 and 9 "are considered obvious as optimization of design parameters." There is no reason to suspect, though, that an ordinarily skilled person would have considered the resistivity of the substrate where the surge absorption element and its transistor are fabricated to be a parameter that should be maximized in order to conserve space on the substrate (see claim 8 and 10). Nor is there any reason to suspect that an ordinarily skilled person would have known what parameters to maximize in order to minimize the area on the substrate needed by the surge absorption element (claims 9 and 11).

For the foregoing reasons, it is respectfully submitted that this application is in condition for allowance. Reconsideration of the application is therefore respectfully requested.

Respectfully submitted,



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